

What is Claimed is:

1 1. A split gate flash memory cell, comprising:
2 a substrate having a trench;
3 a conductive stud disposed in the lower trench and
4 insulated from the substrate serving as a source line;
5 a source region formed in the substrate adjacent to the
6 upper conductive stud;
7 an insulating layer disposed on the conductive stud;
8 a conductive spacer disposed on the upper sidewall of the
9 trench serving as a floating gate, protruding and insulated from
10 the substrate;
11 a first insulating stud disposed on the insulating layer,
12 with the top thereof higher than that of the conductive spacer;
13 a first conductive layer disposed over the substrate of the
14 outside conductive spacer serving as a control gate, the first
15 conductive layer insulated from the conductive spacer and the
16 substrate, respectively;
17 a first insulating spacer disposed on the sidewall of the
18 insulating stud to cover the first conductive layer; and
19 a drain region formed in the substrate of the outside first
20 conductive layer.

1 2. The memory cell as claimed in claim 1, further comprising
2 a second conductive layer disposed between the first conductive
3 layer and the first insulating spacer.

1 3. The memory cell as claimed in claim 2, wherein the second
2 conductive layer is tungsten silicide.

1 4. The memory cell as claimed in claim 1, further comprising
2 a second insulating spacer disposed on the sidewall of the first
3 conductive layer.

1 5. The memory cell as claimed in claim 4, wherein the first
2 and second insulating spacers are silicon nitride.

1 6. The memory cell as claimed in claim 1, further
2 comprising:
3 a conductive plug disposed on the drain region serving as
4 a bit line contact;
5 a cap layer disposed over the insulating stud and the first
6 insulating spacer; and
7 a third conductive layer serving as a bit line disposed on
8 the conductive plug and the cap layer.

1 7. The memory cell as claimed in claim 6, wherein the
2 conductive plug is doped polysilicon.

1 8. The memory cell as claimed in claim 6, wherein the cap
2 layer is silicon oxide.

1 9. The memory cell as claimed in claim 6, wherein the third
2 conductive layer is tungsten.

1 10. The memory cell as claimed in claim 1, wherein the
2 conductive stud is polysilicon.

1 11. The memory cell as claimed in claim 1, wherein the
2 insulating layer is high density plasma oxide.

1 12. The memory cell as claimed in claim 1, wherein the
2 conductive spacer is doped polysilicon.

1 13. The memory cell as claimed in claim 1, wherein the
2 insulating stud is silicon oxide or boron silicate glass.

1 14. The memory cell as claimed in claim 1, wherein the first
2 conductive layer is polysilicon.

1 15. A split gate flash memory cell, comprising:
2 a substrate having a trench;
3 a polysilicon stud disposed in the lower trench and
4 insulated from the substrate serving as a source line;
5 a source region formed in the substrate adjacent to the
6 upper polysilicon stud;
7 an insulating layer disposed on the polysilicon stud;
8 a polysilicon spacer disposed on the upper sidewall of the
9 trench serving as a floating gate, protruding and insulated from
10 the substrate;
11 an insulating stud disposed on the insulating layer, with
12 the top thereof higher than that of the polysilicon spacer;
13 a polysilicon layer disposed over the substrate of the
14 outside polysilicon spacer serving as a control gate, with the
15 polysilicon layer insulated from the polysilicon spacer and the
16 substrate, respectively;
17 a first insulating spacer disposed on the sidewall of the
18 first insulating stud to cover the polysilicon layer;
19 a second insulating spacer disposed on the sidewall of the
20 polysilicon layer; and

21 a drain region formed in the substrate of the outside
22 polysilicon layer.

1 16. The memory cell as claimed in claim 15, further
2 comprising a tungsten silicide layer disposed between the
3 polysilicon layer and the first insulating spacer.

1 17. The memory cell as claimed in claim 15, wherein the
2 first, second, and third insulating spacers are silicon nitride.

1 18. The memory cell as claimed in claim 15, further
2 comprising:

3 a polysilicon plug disposed on the drain region serving as
4 a bit line contact;

5 a cap layer disposed over the insulating stud and the first
6 insulating spacer; and

7 a tungsten layer serving as a bit line disposed on the
8 polysilicon plug and the cap layer.

1 19. The memory cell as claimed in claim 18, wherein the cap
2 layer is silicon oxide.

1 20. The memory cell as claimed in claim 15, wherein the
2 insulating layer is high density plasma oxide.

1 21. The memory cell as claimed in claim 15, wherein the
2 first insulating stud is silicon oxide or boron silicate glass.